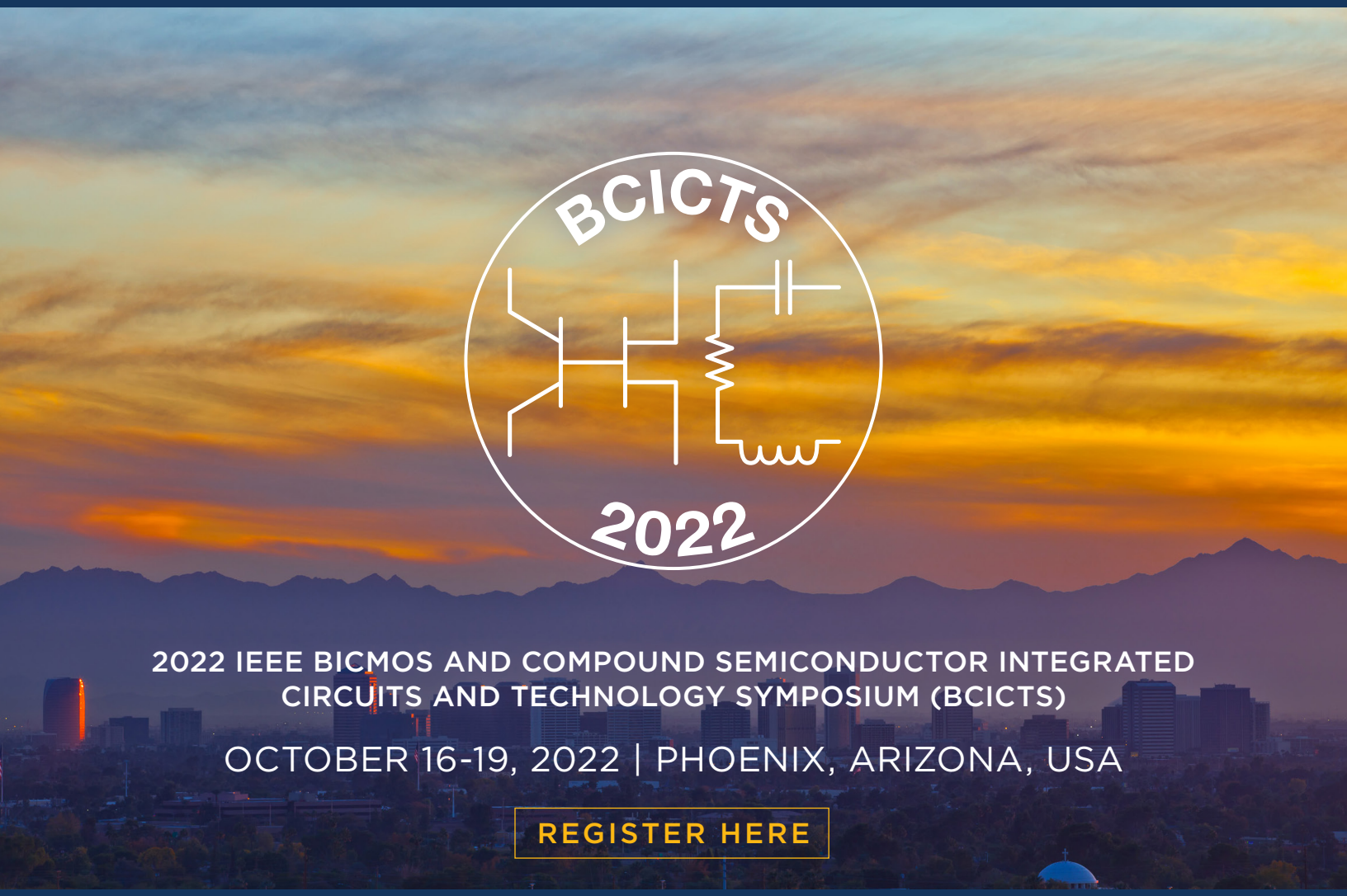

2022 IEEE BICMOS AND COMPOUND SEMICONDUCTOR INTEGRATED CIRCUITS AND TECHNOLOGY SYMPOSIUM (BCICTS)

OCTOBER 16-19, 2022 | PHOENIX, ARIZONA, USA

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MILLIMETER-WAVE AND THZ APPLICATIONS – SYSTEMS, CIRCUITS, DEVICES AND TECHNOLOGIES

SUNDAY OCTOBER 16, 2022 • 8:30AM - 5:30PM

Millimeter-Wave Sensing – Circuits, Systems and Applications
Instructor: Dr. Arun Paidimarri, IBM T.J. Watson Research Center

Circuit Design for Millimeter-Wave Applications in Communication and Sensing
Instructor: Prof. John R. Long, University of Waterloo, Canada

SiGe BiCMOS technology for mm-wave and THz applications
Instructor: Dr. Pascal Chevalier, STMicroelectronics

InP technology for mm-wave and THz applications
Instructor: Dr. Miguel Urteaga, Teledyne Scientific Company

Millimeter-Wave Sensing – Circuits, Systems and Application

Instructor: Dr. Arun Paidimarri, IBM T.J. Watson Research Center

ABSTRACT

The development and progression of phased array systems for communications and sensing has accelerated with mmWave 5G. High-performance phased arrays have been demonstrated at frequencies up to 60-GHz with research prototypes going all the way up to 300GHz. These devices promise to enable new sensing applications co-existing with communications in the context of 6G systems. In this talk, we present phased array architectures and examples of how they are integrated at the system level to enable sensing applications. We also present digital control architectures that are necessary to orchestrate the sensing in concert with the baseband signals. We then present three example applications of sensing using some of the phased array systems developed at IBM Research.

We describe a high-speed 3D radar data acquisition system operating at 60GHz with a16-element phased array. It is engineered to acquire 100s of frames per second using 1 GHz of bandwidth and scanning across 441 directions. An AI algorithm is then trained to automatically recognize events using the 3D radar data. Two use cases are presented: (1) hand gestures classification, and (2) classification of concealed objects in motion.

We demonstrate a multi-spectral imaging platform “hyperimager” consisting of sensors, an App, and cloud infrastructure. The sensors include the 3D radar system at 60GHz, IR and visible-domain information. The system is able to capture multi-spectral images that can exploit the advantages of each domain. We also demonstrate a joint communications and 3D sensing application using IBM’s Software Defined Phased Array Radio (SDPAR). The SDPAR uses a state-of-the-art 28GHz 64-element phased array in conjunction with a SDR and a common API to ease system development of applications using phased arrays. 3D sensing is obtained by time-of-flight measurement using OFDM waveforms that are already in use for communications. A total of 1GHz of sensing bandwidth is obtained by stitching 100MHz wide packets across time. Such a joint sensing-communication doesn’t affect underlying communication bandwidth.

We finally present a scalable, Software-Defined, Platform for <6-GHz and 28-GHz RF data collection, storage, and analysis. The system enables high-speed ingestion of I/Q data streams, large storage and APIs to easily consume and analyze data, and compute architecture for running algorithms including AI/ML. The system could thus be utilized for running many of system ideas described in this talk and provides a platform for developing many more in the future.

ABOUT YOUR INSTRUCTOR

Arun Paidimarri received the B.Tech degree in electrical engineering from the Indian Institute of Technology, Bombay, India, in 2009 and the S.M. and Ph.D degrees in electrical engineering and computer science from the Massachusetts Institute of Technology (MIT), Cambridge, MA in 2011 and 2015 respectively. He is currently a Research Staff Member at the IBM T.J. Watson Research Center, Yorktown Heights, NY. His research interests are in low power wireless system design, mm-wave circuit design and software-defined phased arrays. He is a member of the technical program committees for RFIC Symposium and BCICTS. Dr. Paidimarri is a co-recipient of the best-paper awards at the IEEE International Conference on Communications (ICC) 2013 and at SmartCom 2019. He was awarded the President of India Gold Medal in 2009. He won a Silver Medal at the 37th International Chemistry Olympiad held in Taipei, Taiwan in 2005.

Circuit Design for Millimeter-Wave Applications in Communication and Sensing

Instructor: Prof. John R. Long, University of Waterloo, Canada

ABSTRACT

Millimeter-wave front-end circuits employed in communication and sensing applications are described in this lecture. Typical circuit blocks and their design are presented and analyzed. These include: low-noise amplifiers (LNAs), T/R switches, phase shifters, voltage-controlled oscillators (VCOs and DCOs), frequency multipliers, mixers, and power amplifiers (PAs). The performance of lumped-element varactors, inductors, and transformers integrated on-chip and used in the design and optimization of these circuits is also reviewed. Scaling and modeling of on-chip passives for application in VCO/DCO resonators, low-loss feedback networks, baluns, power combiners/splitters, biasing and peaking networks are discussed. Circuit impairments caused by physical layout and back-end technology constraints at mm-wave frequencies are highlighted. Finally, substrate shielding methods, which is essential to reduce substrate losses (esp. for silicon) at mm-wave frequencies, are also described.

ABOUT YOUR INSTRUCTOR

John R. Long received the B.Sc. from the University of Calgary in 1984, and the M.Eng. and Ph.D. degrees in Electronics Engineering from Carleton University in Canada in 1992 and 1996, respectively. He has worked at Bell-Northern Research Ltd. (Ottawa), the University of Toronto (1996-2001), and the Delft University of Technology in the Netherlands (2002-2014). In January 2015 he joined the ECE Department at the University of Waterloo in Canada. His current research interests include low-power transceiver circuitry for highly integrated radio and high-speed data communication applications. He is an IEEE Fellow and is currently president of the IEEE Solid-State Circuits Society.

SiGe BiCMOS technology for mm-wave and THz applications

Instructor: Dr. Pascal Chevalier, STMicroelectronics

ABSTRACT

SiGe BiCMOS technology enjoys a continuous improvement of Silicon Germanium (SiGe) Heterojunction Bipolar Transistor (HBT) performance combined nowadays with nanoscale CMOS nodes (90nm an below). It allowed accompanying the Ethernet communication roadmap (from few Gb/s to several hundred of Gb/s today) and serving millimeter-wave applications for wireless infrastructures and automotive radars. Today we are discussing the use of SiGe for the 6th generation of mobile communication, including at sub-THz frequencies.

This lecture will start with a review of the figures of merits, assets and state-of-the-art of SiGe BiCMOS, and its positioning versus other competing technologies. Vertical and lateral scaling principles and the related trade-offs driving the choice of the SiGe HBT device architecture will be presented after a reminder on device physics basics. Next, performance of CMOS and passive devices will be exhibited along with the related integration challenges using STMicroelectronics' technologies example.

Finally, the capability of SiGe BiCMOS to address THz applications will be discussed. It will be shown that a low-cost transceiver enabling a 100 Gb/s link at 150 GHz can be fabricated in a 55-nm SiGe BiCMOS technology. Perspectives to address applications above 300 GHz will also be debated in the perspective of the BiCMOS roadmap.

ABOUT YOUR INSTRUCTOR

Pascal Chevalier received the Ph.D. degree in electronics from the University of Lille, France, in 1998 for his work on InP-based HEMT. He joined Alcatel Microelectronics, Belgium, in 1999, where he contributed to the start of RF BiCMOS. Since joining STMicroelectronics, Crolles, France, in 2002, he has been working on the development of SiGe BiCMOS and RF-SOI CMOS technologies and related devices, with a long-lasting research interest in SiGe HBT. He is currently leading the RF-SOI CMOS, BiCMOS & Disruptive Technologies R&D team and is a Senior Member of Technical Staff. Dr. Chevalier has authored or co-authored over 200 technical journal papers and conference publications. He has served the Technical Program Committees of the IEEE Bipolar / BiCMOS Circuits and Technology Meeting (BCTM) and the ECS SiGe Symposium. He has been a member of the RF & AMS Technologies section of the ITRS of which he led the Silicon Bipolar & BiCMOS subgroup. He currently serves the Technical Program Committees of the IEEE Bipolar and Compound Semiconductor Integrated Circuits and Technology (BCICTS) and the IEEE International Electron Devices Meeting (IEDM).

InP technology for mm-wave and THz applications

Instructor: Dr. Miguel Urteaga, Teledyne Scientific Company

ABSTRACT

Future mm-Wave and sub-THz communication systems seek to exploit the large available spectral bandwidth at frequencies >100GHz. Large-element MIMO array architectures envisioned for these systems will require high-performance and high-efficiency frontend elements (power amplifiers, low-noise amplifiers…). Indium phosphide (InP) transistor technologies have demonstrated THz-class device bandwidths. Presently, at frequencies >100GHz, InP-based high electron mobility transistor (HEMT) technologies offer the highest performance low noise amplifiers (LNAs) and InP heterojunction bipolar transistor technologies (HBTs) offer the highest performance power amplifiers (PAs). In this short course, the design and performance of InP HBTs will be reviewed with an emphasis on technology considerations for mm-Wave power amplifier design. InP HBT performance is strongly influenced by non-equilibrium (ballistic) transport effects in the collector and the modeling and impact of these effects on circuit operation will be discussed. Power amplifier results in InP HBT technologies from 100-300GHz will be presented and prospects for improving PA efficiency and output power density will be considered. Finally, techniques that have been demonstrated for the heterogeneous integration of InP technologies with Si technologies will be reviewed.

ABOUT YOUR INSTRUCTOR

Miguel Urteaga received his M.S. and Ph.D. degrees in Electrical Engineering from the University of California Santa Barbara in 2001 and 2003, respectively. He is currently the director of Foundry Products and Services for Teledyne Scientific Company and manages the advanced device development group. His research is focused on the development of ultra-high speed transistor technologies, primarily in the InP material system. He has led the development of Teledyne's high performance InP HBT IC technologies. These technologies have been used to demonstrate state-of-the-art integrated circuits ranging from high-speed mixed-signal and digital ICs to mm-wave and THz monolithic integrated circuits. He served as the program manager at Teledyne for the DARPA THz Electronics, Diverse Accessible Heterogeneous Integration (DAHI) and Dynamic Range-enhanced Electronics Materials (DREAM) programs. He has authored or co-authored over 200 conference and journal publications.

BCICTS PRIMER

SIMULATION METHODS AND TOOLS FOR RF DESIGN

SUNDAY OCTOBER 16, 2022 • 8:30AM - 12:30PM

ABSTRACT

This primer course was developed to serve as an introductory-level course on simulation methods commonly used in RF and MMW integrated circuit design.

Covered material includes:

- Classical circuit simulation principles and requirements for compact models, substrate [and thermal] effects
- Non-linear circuit simulation principles and applications (time, frequency, and mixed frequency-time methods)
- LTI and LPTV small signal analyses and applications
- Modeling distributed structures for circuit simulation (EM simulation)
- Parasitic extraction and reduction
- Examples/Case-studies

ABOUT YOUR INSTRUCTOR

Kiran K. Gullapalli received the B.Tech. degree in electrical engineering from the Indian Institute of Technology Madras, Chennai, India, in 1989, and the M.S. and Ph.D. degrees in electrical and computer engineering and the M.B.A. degree from the University of Texas at Austin, Austin, TX, USA, in 1991, 1994, and 2009, respectively. He joined Circuit Simulation Group, Motorola, Austin, TX, USA, in 1994 and has been working on various aspects of circuit simulation ever since. He worked on Motorola's in-house circuit simulator, Mica, with a focus on device models and RF simulation. In 2002, he joined Synopsys, Mountain View, CA, USA, where he worked on fast-SPICE techniques. In 2005, he re-joined the Mica Circuit Simulation Group at NXP, Austin, where he continues to work on high performance Analog and RF simulation. In 2017 he was elected NXP fellow for his contributions to Analog and RF simulation.
